	L #	Hits	Search Text	DBs
1	L2	34	((detect$3 determin$3 diagnos$3 identif$6) near10 instruction) near99 ((configuration adj2 (data memory))) and cpu	USPAT; US-PGPUB
2	L1	34	((detect$3 determin$3 diagnos$3 identif$6) near10 instruction) near99 ((configuration adj2 (data memory))) and cpu	USPAT; US-PGPUB

the generate (G), propagate (P), carry in and carry out leads to carry look ahead circuitry will be described hereinbelow with respect to the configuration control of the local processors. An indication of the sign of either the 18-bit or 36-bit value computed is provided in a conventional manner by connections to the appropriate sign digits from the accumulator.

As previously discussed, the DACT and DACF fields of the micro control word in the control store 36 selectively provide, in accordance with decision point 11, addresses into a deferred action control table in the control circuits 41 for controlling the performance of global deferred actions. Referring now to FIG. 7, deferred action control table 106 is illustrated. The deferred action control table 106 comprises a memory for storing a plurality of words addressed in accordance with DACT and DACF, the bits thereof providing a master bitted list of the actions to be performed. For example, the memory 106 includes 28 words of 22 bits each where each bit controls a particular action. The bit outputs from the memory 106 are connected to the appropriate control circuitry for effecting the designated actions in accordance with the states of the bits. For example, bit 0 which controls the action P→IAR controls the transfer of the contents of the program counter 31 to the instruction address register 12 by connecting the bit 0 output from the memory 106 to the strobe input of the register 12. Thus, when a word is addressed in the memory 106 at either the address DACT or DACF selectively under control of DP 11; if bit 0 of that word is set to 1, the P→IAR transfer will take place, otherwise it will not. In a similar manner, the other bits of the memory 106 are connected to the components designated by the particular action listed to control the deferred action associated therewith. Details of the control connections will be later described. Thus, the two control store fields DACT and DACF specify the particular deferred action choices for a micro instruction. The table 106 includes a word for each combination of deferred actions desired. Several deferred actions will occur simultaneously if several bits are set in the words read from the memory.

The choice as to whether the word in the memory 106 addressed by the DACT field or that addressed by the DACF field is utilized is controlled by the state of DP 11. This selection is implemented by utilizing two identical memories, one addressed by DACT and the other addressed by DACF where the corresponding bits from the memory are gated at the device to be controlled in accordance with DP 11. For example, the BRG BIT 0 bits from both the DACT and DACF memories are connected to the least significant stage of the BRG register 66 and the bit from one memory or the other is loaded into that stage under control of DP 11. The details for the selective control of the deferred actions will be described hereinbelow.

Most of the mnemonics specifying the deferred actions to be performed refer to register and latches discussed hereinabove with respect to FIG. 5. For example D→IAR controls placing the value on the D bus 23 into the instruction address register 12. The STORE OP action controls storing the operand in the MDRW register 15 into the main memory at the address in the operand address register (OAR) 14. The FETCH NI action causes fetching of the next macro instruction at the address in the IAR register 12 into the MIR register 13. The LOAD BRG, BRG BIT 0 and BRG BIT 1 actions control the loading of the BRG register 66 with the bits provided by bits 11 and 12 of the memory 106. The STATICIZE action sets a latch in the control circuits 41 called STAT MEM. The output of the STAT MEM latch provides the STAT signal for the staticizer register 56. It should be noted that the D0 and D1 designations refer to the static variables discussed above with respect to Table 4 and that the D→GRS (R) and the D→GRS (L) actions are utilized in loading the right hand or left hand side of the selected register of the general register stack 32 from the D bus 23 respectively, the left hand side (L) referring to the left most 20 bits of the D bus 23 and the right most half (R) referring to the 20 right most bits thereof.

TABLE DRIVEN DECISION LOGIC

As discussed above with respect to FIG. 4, the CPU 10 requires a plurality of decisions to be made to provide for conditional control of the computer. Decision logic 40 (FIGS. 2 and 5) provides 12 decision points DP0-DP11 for effecting the required control in a manner to be described below with respect to FIGS. 8 and 9. The relationships between the decision points and the micro control fields illustrated in FIG. 4 were set forth above where the binary states of the decision points determine the selection. Briefly, (referring to FIG. 9)

DP0—controls the real branching by selecting either address NAT or NAF in accordance with a function selected by JDS where address NAT may be modified to perform a vector jump with respect to the class base, the instruction and the interrupt vectors under control of the XF field.

DP1 and DP2—are or'ed with the two least significant bits of address NAT respectively to effect a 4-way conditional vector branch. The logic functions that provide DP1 and DP2 are selected by fields VDS0 and VDS1 respectively.

DP3-DP6—select between the LPFT and LPFF function control fields for the respective processors P1-P4 in accordance with logic functions selected by the PDS fields respectively. These decision points control the phantom branching of the CPU 10 in a manner to be described.

DP7-DP10—provide deferred action conditional control for the respective local processors P1, P2, P3 and P4 in accordance with logic functions selected by the respective DDS fields. These decision points are utilized in conjunction with the OUT, WLM, WLMA and SCS field to conditionally place the accumulator contents of the local processors, P1, P2 and P3 onto the D bus 23, write into the local memories 24, 25, 26 and 28 and set the static control variables SC1-SC7 as discussed above with respect to Table 4.

DP11—controls the global deferred action by selecting between the DACT and DACF addresses into the deferred action control table of FIG. 7 in accordance with a logic function selected by the DADS field.

Thus, the decisions delineated above are effected by the binary states of the decision points in accordance with the selected logic function. The CPU 10 utilizes 24 static variables and 16 dynamic variables which are selectively applied as the inputs to the logic functions which variables are delineated in Table 4 above. The static variables have values which exist before the start of a micro cycle and may exist over several micro cycles. The dynamic variables are computed during a micro cycle at about t_{67} of the 100 nanosecond cycle

	Document ID	U	Title	Current OR
1	US 20040025121 A1	☐	Method of and apparatus for information processing	716/3
2	US 20040003223 A1	☒	Apparatus and method to decrease boot time and hibernate awaken time of a computer system	713/1
3	US 20030204791 A1	☒	Rules-based configuration problem detection	714/48
4	US 20030056128 A1	☒	Apparatus and method for a selectable Ron driver impedance	713/300
5	US 20030036874 A1	☒	Network-based system for configuring a measurement system using configuration information generated based on a user specification	702/123
6	US 20030005104 A1	☒	Server configuration tool	709/223
7	US 20020157066 A1	☒	Reconfigurable processor devices	716/1
8	US 20020133690 A1	☒	Semiconductor integrated circuit	712/34
9	US 20020016674 A1	☒	Golf course yardage and information system having improved zone information and display characteristics	701/215
10	US 20020011949 A1	☒	Golf course yardage and information system with zone detection	342/357.06
11	US 20020010544 A1	☒	Display monitor for golf cart yardage and information system	701/213
12	US 6728723 B1	☒	Method and system for verifying configuration transactions managed by a centralized database	707/102
13	US 6597666 B1	☒	Method, editor, computer, control module, and storage means for editing configuration data for telecommunications systems	370/254
14	US 6553395 B2	☒	Reconfigurable processor devices	708/232
15	US 6525690 B2	☒	Golf course yardage and information system with zone detection	342/357.13
16	US 6470242 B1	☒	Display monitor for golf cart yardage and information system	701/1
17	US 6421817 B1	☒	System and method of computation in a programmable logic device using virtual instructions	716/16
18	US 6353841 B1	☒	Reconfigurable processor devices	708/232
19	US 6351797 B1	☒	Translation look-aside buffer for storing region configuration bits and method of operation	711/207

GWA fields from the control store 36 are applied as the selection inputs to the multiplexer 77 and 78 respectively. Additionally, a write enable flip-flop 79 responsive to timing signals t_0 and t_{50}, which timing signals will be later described, applies control signals to the chip enable inputs of the multiplexers 77 and 78 to provide the timing for the GRS writing and reading operations.

In a manner to be further described hereinbelow, the CPU 10 operates with a 100 nanosecond micro cycle, timing strobes being provided every ten nanoseconds, the strobes being designated as t_0–t_{90}. Thus, it is appreciated that at t_0 the write enable flip-flop 79 is set and at t_{50} it is reset. Thus, during the first half of the micro cycle the multiplexer 78 is enabled for writing and during the second half of the micro cycle the multiplexer 77 is enabled for reading. Thus, in accordance with the GRA and GWA fields from the micro instruction words, one of the four input addresses is selected by the GWA field during the first half of the micro cycle and is transmitted through the OR gate 76 to address the GRS 32 for writing. During the second half of the micro cycle one of the four input addresses is selected by the GRA field and transmitted through the OR gate configuration 76 to address the GRS 32 for reading. RAR1 usually contains the absolute address of the register pointed at by the a field of the macro instruction, which value is generally computed toward the beginning of the macro instruction emulation by the local processor 27. The RAR1 register receives this address from the 7 least significant bits from the D4 bus 30. The RAR2 register is usually utilized to contain the address of A_a+1 for the 1108 double precision instructions and receives this address information from the 7 least significant bits of the D4 bus 30. The register RAR3 usually contains the GRS address provided by the u field of the macro instruction which, in accordance with 1108 addressing, is the 'hidden' memory. Any of the local processors 17, 18 and 19 may provide the computations to provide this address information to RAR3 which is taken from the right 7 of the left 20 bits of the 40-bit wide D bus 23. The fourth address source is provided directly from the macro instruction register 13 by the x field concatenated with the D6 bit. D6 determines whether the x register is in the user state or in the executive state in a manner identical to that utilized in the 1108. Because of the boundaries chosen by the 1108, the D6 bit can merely be concatenated in a manner to be described hereinbelow.

The addressing for the GRS was generally discussed above with respect to Tables 3 and 9 from which it is appreciated that the base address computations are performed by the local processor 27 in response to the GB field from the IST memory 38, the results being provided to the register address registers 33 as directed by the GRA and GWA fields in the micro instructions in the control store 36.

As previously discussed, the CPU 10 includes local processors 17, 18 and 19 designated as P1, P2 and P3 which have local memories 24, 25 and 26 associated therewith respectively. Each of the local memories 24, 25 and 26 are 64 words long by 40 bits wide. The local memory 24 is addressed by a 6-bit, 3 input multiplexer 80 where the inputs are selected by the LMAS field from the local control field associated with the processor P1 provided from the control store 36 as discussed above with respect to Table 5. One of the inputs to the multiplexer 80 is provided by the LMA field from the local control field associated with the processor P1 whereby the local memory 24 may be addressed directly under micro program control. A second input to the multiplexer 80 is provided from a local memory address register (LMAR) 81 which is loaded from the 6 least significant bits of the D bus 23 under control of the deferred action control table in the control circuits 41. Thus, in a manner to be described hereinafter, the local memory 24 may be addressed in accordance with a deferred action. The third input to the multiplexer 80 is provided from the shift/mask address PROM 70 which addresses thirty-six locations in the local memory 24 which are utilized for storing masks used in the local processor computations.

The addressed words from the local memory 24 are applied through a complementary 82 to an A latch register 83 which, in turn, provides its 40-bit input to the A port of the local processor 17. The complementer 82 will transmit the addressed word from the local memory 24 to the A register 83 in either an uncomplemented or complemented form in accordance with inputs LMAS, MC and SE thereto. It is appreciated that the control field LMAS is provided from the control store 36, the field MC from the instruction status table 38 and the field SE from the associated static variable flip-flop in the control circuits 41 as indicated above with respect to Table 4. The detailed control of the complementer 82 will be later discussed. The latches provided by the A register 43 are required since the A port of the local processor 17 is not provided with an internal latch. The B port to the local processor 17 is so provided. The selective complementation control of the complementer 82 is primarily utilized in mask extraction from the local memory 24 under control of the shift/mask address PROM 70 so that 36 masks as well as their complements may be selectively provided from the local memory 24 as indicated above with respect to Tables 5 and 12.

The input, output, arithmetic and logic function control for the local processor 17 is provided by 16 function bits S_0–S_{15}. In a manner to be later described in greater detail, the local processor 17 has a useful repertoire of approximately 67 functions, the 16-bit function code selecting the functions by utilizing a semi-master-bitted approach. Fourteen of the 16 function bits, namely $S_{0\text{-}3, 5\text{-}7, 9\text{-}15}$ are provided from a 2 input multiplexer 84 via a function latch 85. The 2 inputs to the multiplexer 84 are provided from the control store 36 by the LPFT and LPFF fields of the portion of the micro control word associated with the local processor P1. The selection of these function control fields is provided by the selection input to the multiplexer 84 from decision point 3 from the decision logic 40. Thus, in accordance with the state of DP3, either the function called for by the LPFT or that called for by LPFF will be performed by the local processor 17 in accordance with the control arrangement for the CPU 10 to be later described.

The S_8 function bit of the local processor 17 controls the output of the local processor accumulator to the D port. The S_8 function bit is provided from an accumulator output control multiplexer 86 via an S_8 function latch 87. The 2 bits of the OUT field of the portion of the micro control word associated with the P1 processor are applied respectively to the 2 inputs to the multiplexer 86, selection therebetween being effected by the decision point 7 signal from the decision logic 40. The specific output control effected was delineated above with respect to Table 8. For reasons to be clarified, the local processor function controlled by the S_4 function

	Document ID	U	Title	Current OR
20	US 6289396 B1	☒	Dynamic programmable mode switching device driver architecture	719/323
21	US 6236940 B1	☒	Display monitor for golf cart yardage and information system	701/300
22	US 6236360 B1	☒	Golf course yardage and information system	342/357.13
23	US 6172521 B1	☒	Programmable logic IC having memories for previously storing a plurality of configuration data and a method of reconfigurating same	326/40
24	US 6065067 A	☒	System, method and program for controlling access to an input/output device possible resource settings data in an advanced configuration and power interface operating system	710/8
25	US 6047115 A	☒	Method for configuring FPGA memory planes for virtual hardware computation	716/16
26	US 5878369 A	☒	Golf course yardage and information system	701/215
27	US 5860133 A	☒	Method for altering memory configuration and sizing memory modules while maintaining software code stream coherence	711/171
28	US 5752035 A	☒	Method for compiling and executing programs for reprogrammable instruction set accelerator	717/153
29	US 5748979 A	☒	Reprogrammable instruction set accelerator using a plurality of programmable execution units and an instruction page table	712/37
30	US 5689431 A	☒	Golf course yardage and information system	701/213
31	US 5179530 A	☒	Architecture for integrated concurrent vector signal processor	708/520
32	US 4989137 A	☒	Computer memory system	711/203
33	US 4967340 A	☒	Adaptive processing system having an array of individually configurable processing components	712/19
34	US 4775932 A	☒	Computer memory system with parallel garbage collection independent from an associated user processor	707/206

bit is not utilized in the operation of the CPU 10 and the function is disabled by applying a permanent "1" signal to the S_4 input. The components 80, 82–87 may for convenience be designated as a block 88.

Associated with the local processor 18 and local memory 25 is a block 88' and associated with the local processor 19 and the local memory 26 is a lock 88". The blocks 88' and 88" are identical to the block 88 with the exception that appropriately associated local control fields from the control store 36 are applied thereto. The local memory address register 81 and the shift/mask address PROM 70 provide inputs to the blocks 88' and 88" for reasons similar to those discussed with respect to the block 88.

The local processor 27 with its associated local memory 28 is configured somewhat differently from the processor 17, 18 and 19. The addressing of the local memory 28 has previously been discussed with respect to the blocks 63 and 64. The local processor 27 utilizes 16 function bits S_0–S_{15} in a manner similar to that described above with respect to the processor 17. The function bits $S_{0-3, 5-7, 9-15}$ are provided in parallel from a function select multiplexer 89 via a function latch 90. The 2 inputs to the multiplexer 89 are provided from the control store 36 by the local processor function fields LPFT and LPFF from the portion of the micro control word associated with the P4 processor as discussed above with respect to FIG. 4. The selection between LPFT and LPFF is effected by decision point 6 from the decision logic 40. The carry in (C_{IN}) input to the processor 27 is treated as a function bit and is provided from one of the function bit outputs of the multiplexer 89. The S_8 input is permanently enabled by a 1 input since the processor 27 utilizes the private D_4 bus 30 to which it exclusively provides inputs. The S_4 input to the processor 27 is permanently disabled in the manner and for the reasons discussed above with respect to the processor 17.

Each of the local processors 17, 18, 19 and 27 are preferably constructed from LSI chips of the micro processor variety. Particularly, the Motorola 10,800 4-bit slice ALU was selected for the implementation. The detailed specifications for this ALU slice may be found in the publication entitled "M10800-HIGH PERFORMANCE MECL LSI PROCESSOR FAMILY", 1976, available from Motorola Semiconductor Products, Inc. It should be noted that the terminology utilized herein, namely, A bus, B bus and D bus, corresponds to the Motorola terminology A bus, O bus and I bus respectively.

Referring now to FIG. 6, a schematic block diagram of the ALU slice utilized to implement the local processors 17, 18, 19, and 27 is utilized depicting the components and paths that are utilized in the CPU 10. The input from the A register 83 (FIG. 5) to the A port is applied as an input to a multiplexer 100 whose output is applied to the ALU 101 of the chip as well as to a mask network 102. Another input to the mask network 102 is provided from a B bus latch 103 utilized to latch values from the B bus 22 (FIG. 5) at the beginning of each micro cycle. The output of the mask network 102 as well as the output from the latch 103 provide inputs to the ALU block 101. The ALU 101 receives the 16 function select bits S_0–S_{15} as discussed above as well as a carry in signal. The ALU 101 also provides carry generate (G), carry propagate (P), as well as overflow and carry out signals.

The output from the ALU 101 is applied to a 1-bit shifter 104 whose output is applied to a micro accumulator 105 (designated as α) whose output, in turn, provides the value to the output D port of the processor. The output of the accumulator 105 is also applied as an input to the A bus multiplexer 100, the B bus latch 103 and the ALU 101. The shifter 104 includes a bi-directional port for the least significant bit (LSB) as well as a bi-directional port for the most significant bit (MSB) and also provides a ZERO detect output utilized as a dynamic variable in the CPU 10 which provides an indication when all of the bits transmitted through the shifter are 0.

The chip illustrated in FIG. 6 provides Boolean logic functions, binary arithmetic and a set of data routing functions, the chip having a repertoire of approximately 67 functions. As discussed above, the functions are selected by the semi-master-bitted inputs S_0–S_{15}. As previously described, the D port output can be disabled by the function bit S_8 permitting the wired OR output to the D bus 23. The basic arithmetic repertoire is add, subtract, complement, shift 1 bit and the basic logic repertoire is AND, OR, EXCLUSIVE OR and NOT. Additionally, the chip can perform a Boolean logic function followed by an arithmetic function in the same micro cycle utilizing the mask network 102. Since the shift 104 is constrained to a 1-bit shift per cycle, the external high speed shifter 35 is utilized as described with respect to FIGS. 2 and 5. Data from the B bus 22 is latched in the B bus latch 103 at the beginning of each micro cycle and the result of the last operation is latched in the accumulator 105 at the end of a cycle. Since there is no internal latch for the A port of the chip, the external A register 83 is utilized to provide this capability. The complete repertoire for the chip as well as the details of its structure and operation are documented in said Motorola specification referenced above.

Each of the chips utilized is 4-bit wide and is sliced parallel to the data flow. The chip is expanded to the 40-bits required by the processors 17, 18 and 19 and to the 20-bits required by the processor 27 by connecting the circuits in parallel. Specifically, in implementing the local processors 17, 18 and 19, 10 4-bit wide chips such as illustrated in FIG. 6 are utilized with the resulting 40-bit wide A, B, and D ports connected in parallel to the 40-bit wide A bus register 83, B bus 22 and D bus 23 respectively. The local processor 27 is comprised of 5 such chips with the resulting 20-bit wide A, B, and D ports being connected in parallel to the 20-bit wide memory 28, B_4, bus 29 and D_4 bus 30, respectively. For each of the local processors 17, 18, 19 and 27, the function control bits S_0–S_{15} are applied in parallel to all of the chips comprising a processor. The shifter circuits 104 for all of the chips in a processor are serially connected with respect to each other with the MSB shifter output of a chip connected to the LSB of the next higher order chip. The ZERO detect output from the chips comprising a processor are ANDed together to provide the ZERO detect dynamic variable for the processor as delineated above with respect to Table 4. The overflow outputs from the most significant chips of the respective processors 17, 18, 19 and 27 provide inputs to the decision logic 40 as variables into decision logic circuits to be described hereinbelow.

As previously described, the 10 4-bit chips comprising each of the local processors 17, 18 and 19 may be utilized interconnected in a 36-bit mode or as 2, 20-bit processors in the 2×20 bit mode. The connections of